the MOS capacitor and a drain electrode connected to a drain current measuring node (DCMN); and

a fuse with a first end connected to a voltage force node (VFN) and a second end connected to a second electrode of the MOS capacitor and the second end of the fuse also connected to a gate of the MOS transistor.

14. (New) The unit test cell of claim 13, wherein the fuse is a metal line having a smaller width than a wiring line of the unit test cell.

B' (Cont'd)

15. (New) The unit test cell of claim 13, wherein a type of the MOS capacitor is the same as a type of the MOS transistor.

16. (New) The unit cell of claim 15, wherein both the type of the MOS capacitor and the type of the MOS transistor is NMOS.

17. (New) The unit test cell of claim 13, wherein a type of the MOS capacitor is different from a type of the MOS transistor.

18. (New) The unit cell of claim 17, wherein the type of the MOS capacitor is NMOS and the type of the MOS transistor is PMOS.

19. (New) The unit cell of claim 13, wherein a gate oxide film of the MOS transistor is thicker than a dielectric of the MOS capacitor.

20. (New) The unit cell of claim 13, wherein the gate electrode of the MOS transistor is lightly doped such that a voltage applied to the gate electrode is less than the VFN voltage.

21. (New) A method to measure Time to break down (Tbd) of a unit test cell of a Time Dependent Dielectric Breakdown (TDDB) test pattern circuit wherein the unit test cell includes a MOS capacitor with a first electrode connected to ground, a MOS transistor with a source electrode connected to the first electrode of the MOS capacitor and a drain electrode connected to a drain current measuring node (DCMN), and a fuse with a first end connected to a voltage force node (VFN) and a second end connected to a second electrode of the MOS capacitor and the second end of the fuse also connected to a gate of the MOS transistor, the method comprising:

a) applying a stress voltage Vforce to the VFN;

b) applying drain voltage to the DCMN; and

c) measuring current flowing through the DCMN over time.

22. (New) The method of claim 21, further including:

d) noting a point in time where the current flowing through the DCMN drops suddenly.

23. (New) A Time Dependent Dielectric Breakdown (TDDB) test pattern circuit, comprising:

a plurality of unit test cells, each unit test cell includes a voltage force node (VFN) and a drain current measuring node (DCMN), such that all VFNs are commonly connected and all DCMNs are commonly connected.

24. The test pattern circuit of claim 23, wherein each unit test cell further includes:

a MOS capacitor with a first electrode connected to ground;

a MOS transistor with a source electrode connected to the first electrode of the MOS capacitor and a drain electrode connected to the DCMN; and

a fuse with a first end connected to the VFN and a second end connected to a second electrode of the MOS capacitor and the second end of the fuse also connected to a gate of the MOS transistor.

25. (New) The test pattern circuit of claim 24, wherein the fuse is a metal line having a smaller width than a wiring line of the unit test cell.

26. (New) The test pattern circuit of claim 24, wherein a type of the MOS capacitor is the same as a type of the MOS transistor.

27. (New) The test pattern circuit of claim 26, wherein both the type of the MOS capacitor and the type of the MOS transistor is NMOS.

28. (New) The test pattern circuit of claim 27, further comprising:

a substrate pad connecting the MOS capacitor with a bulk electrode of the MOS transistor;

a source pad commonly connecting the source electrodes of MOS transistors;

a VFN pad commonly connecting the VFNs of all unit test cells; and

a DCMN pad commonly connecting the DCMNs of all unit test cells.

29. (New) The test pattern circuit of claim 24, wherein a type of the MOS capacitor is different from a type of the MOS transistor.

30. (New) The test pattern circuit of claim 29, wherein the type of the MOS capacitor is NMOS and the type of the MOS transistor is PMOS.

31. (New) The test pattern circuit of claim 30, wherein a source and drain are formed for each MOS capacitor and further comprising:

a substrate pad connecting the MOS capacitor with a bulk electrode of the MOS transistor;

a first source pad commonly connecting the source electrodes of all MOS transistors;

a second source pad commonly connecting the sources of all MOS capacitors;

a drain pad commonly connecting the drains of all MOS capacitors;

a VFN pad commonly connecting the VFNs of all unit test cells; and

a DCMN pad commonly connecting the DCMNs of all unit test cells.

32. (New) The test pattern circuit of claim 24, wherein a gate oxide film of the MOS transistor is thicker than a dielectric of the MOS capacitor.

33. (New) The test pattern circuit of claim 24, wherein the gate electrode of the MOS transistor is lightly doped such that a voltage applied to the gate electrode is less than the VFN voltage.

34. (New) The test pattern circuit of claim 23, further comprising:

a first voltage source supplying a stress voltage to the VFN of all unit test cells;

a second voltage source supplying voltage to the DCMN of all unit test cells; and

an ammeter connected between the DCMNs and the second voltage source.

35. (New) A method to measure Time to break down (Tbd) of all unit test cells of a Time Dependent Dielectric Breakdown (TDDB) test pattern circuit wherein the test pattern circuit includes a plurality of unit test cells, wherein each unit test cell includes a MOS capacitor with a first electrode connected to ground, a MOS transistor with a source electrode connected to the first electrode of the MOS capacitor and a drain electrode connected to a drain current